UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/615,646	07/13/2000	Josh Hogan	10990815-1	4699

7590 04/20/2004

Hewlett-Packard Company
Intellectual Property Administration
P O Box 272400
Fort Collins, CO 80528-9599

EXAMINER	
BATTAGLIA, MICHAEL V	

ART UNIT	PAPER NUMBER
2652	5

DATE MAILED: 04/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/615,646	HOGAN ET AL.	
	Examiner	Art Unit	
	Michael V Battaglia	2652	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-19 and 21-26* is/are rejected.

7)☒ Claim(s) *20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

disc (Col. 8, lines 41-64); and synthesizing the header information from the recovered address information (Col. 9, lines 12-20).

In regard to claim 3, Kobayashi discloses that the step of synthesizing the header information includes the steps of obtaining address information from the disc (Col. 8, lines 41-64); and synthesizing the header information from the obtained address information (Col. 9, lines 12-20).

In regard to claim 5, Kobayashi discloses that the header information is synthesized by modulation encoding the address information according to a pre-specified format (Col. 6, lines 50-52).

In regard to claims 6 and 7, Kobayashi discloses that the synthesized header information includes a sector address and an error detection code (Col. 6, lines 19-33).

In regard to claim 8, Kobayashi discloses that a combination of analog and digital techniques are used to phase-shift the recovered user data, wherein the voltage controlled oscillator in the PLL circuit (Fig. 14, element 44 in element 41) constitutes the analog technique and the sector counter constitutes the digital technique (Fig. 14, element 46).

In regard to claim 9, Kobayashi discloses that a read clock is used to recover the data; and wherein the recovered data is phase shifted by creating a phase difference between the read clock and the recovered user data (Col. 8, line 65 - Col. 9, line 13).

In regard to claim 14, Kobayashi discloses a read clock for recovering the block from the disc; and wherein the phase difference is inherently faded towards zero according to a time constant related to the read clock (Col. 8, line 65 - Col. 9, line 13). The phase of clock signal produced by the PLL circuit cannot be instantaneously changed to compensate for a phase

difference between the output of the mark detection circuit and the output of the divider. Therefor, the compensation occurs gradually as the phase difference is faded to zero.

In regard to claim 15, Kobayashi discloses a bit-accurate read/write drive for reading a data block from a disc, the drive comprising means for synthesizing header information for the data block (Fig. 14, elements 36-37, 40, and 46); means for recovering actual header information from the disc (Fig. 14, elements 32-33 and 35); and means for recovering actual user data from the disc, the user data being phase-shifted by a phase difference between the synthesized and actual header information (Fig. 14, elements 32-33 and 41 and see Response to Arguments below). The examiner notes that the drive is interpreted as a device that reads data from and/or writes data onto a storage medium.

In regard to claim 16, Kobayashi discloses an apparatus for reading a block of data block from an optical disc, the apparatus comprising an optical pickup unit (Figure 14, element 32); an address detector (Figure 14, elements 33-34); a data recovery circuit for recovering data from an output of the optical pickup unit, the recovered data including actual header information and actual user data of the data block (Figure 14, element 33); a first circuit for synthesizing header information for the data block (Fig. 14, elements 36-37, 40, and 46); a second circuit for determining a phase difference between the recovered actual and synthesized header information (Fig. 14, element 41); and a third circuit for phase-shifting the recovered user data by the determined phase difference (Figure 14, element 33 and see Response to Arguments below).

In regard to claim 17, Kobayashi discloses that the first circuit synthesizes the header information by recovering address information from a wobble embossed on the disc and synthesizing the header information from the recovered address information (Fig. 14, elements 35-36 and 40 and Col. 8, lines 44-51).

In regard to claim 18, Kobayashi discloses that address information is contained on the disc; and wherein the first circuit synthesizes the header information from the address information contained on the disc (Fig. 14, elements 35-36 and 40 and Col. 8, lines 44-51).

In regard to claim 21, Kobayashi discloses that the data recovery circuit includes a read clock (Figure 14, element CLOCK and Col. 9, lines 12-13) and wherein the recovered actual data is phase-shifted by creating a phase difference between the read clock and the recovered actual user data (Col. 8, line 65 - Col. 9, line 11).

In regard to claim 26, Kobayashi discloses an apparatus for correcting a signal recovered during a read operation on a data block stored on a disc, the recovered signal including actual header information and actual user data of the data block (Col. 8, lines 34-40), the apparatus comprising a first circuit for synthesizing header information for the data block (Fig. 14, elements 36-37, 40, and 46); a second circuit for determining a phase difference between the recovered and synthesized header information (Fig. 14, element 41); and a third circuit for phase-shifting the recovered user data by the determined phase difference (Figure 14, element 33 and see Response to Arguments below).

Claim Rejections - 35 USC § 103

3. Claims 4 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi in view of Honma (US 5,917,794).

Kobayashi discloses the method and apparatus for reading a block of data from an optical disc wherein header information is synthesized from address information obtained on the disc by a first circuit as claimed in claims 1, 3, 16, and 18. Kobayashi does not disclose that multiple candidates are synthesized from the address information by a second circuit; wherein a phase

difference between the actual header information and a best candidate is determined; and wherein the recovered user data is shifted according to the determined phase difference. The examiner notes that Kobayashi disclose using a disc that contains header information, address information, and user data (Fig. 7 and 17).

Honma discloses a method and apparatus for reading a block of data stored on an optical disc comprising synthesizing information for a data block by a first circuit (Fig. 4, element 42 and Fig. 5, element 42-1), recovering actual information from the disc by a data recovery circuit (the output of the data recovery circuit is shown by Fig. 4, element x), determining a phase difference between the recovered information and the synthesized information by a second circuit (Fig. 4, element 42), the data being phase-shifted by a phase difference between the synthesized and recovered information by a third circuit (Fig. 4, element 44). The examiner notes that the method and apparatus of Honma would synthesize header information from a data block on the disc of Kobayashi because all of the information read from the disc, which would include header information, is synthesized. Honma further discloses synthesizing multiple candidates from the information, which would include address information contained on the disc of Kobayashi; wherein a phase difference between the actual information, which would include header information contained on the disc of Kobayashi, and a best candidate is determined by the second circuit (Col. 5, lines 14-17 and 41-61); and wherein the recovered information, which would include user data contained on the disc of Kobayashi, is shifted according to the determined phase difference (Col. 5, lines 27-35). In addition, Honma teaches that use of maximum likelihood detectors that select a best candidate from multiple candidates will lead to lead to a lower error rate of information detection (Col. 1, lines 26-45).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to synthesize multiple candidates from the address information recovered from the disc in the method and apparatus of Kobayashi and to shift the recovered user data according to the phase difference between the actual information, including header information, and a best candidate as taught by Honma, the motivation being to detect information on a disc with a low error rate.

4. Claims 10 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi in view of Honma.

Kobayashi discloses the method and apparatus for reading a block of data from an optical disc wherein a read clock is used to recover the data; and wherein the recovered data is phase shifted by creating a phase difference between the read clock and the recovered user data as claimed in claims 1, 9, 16, and 21. Kobayashi does not disclose that the recovered data is phase shifted by time-delaying the recovered data.

Honma discloses a method and apparatus for reading a block of data stored on an optical disc comprising synthesizing information for a data block by a first circuit (Fig. 4, element 42 and Fig. 5, element 42-1), recovering actual information from the disc by a data recovery circuit (the output of the data recovery circuit is shown by Fig. 4, element x), determining a phase difference between the recovered information and the synthesized information by a second circuit (Fig. 4, element 42), the data being phase-shifted by a phase difference between the synthesized and recovered information by a third circuit (Fig. 4, element 44). The examiner notes that the method and apparatus of Honma would synthesize header information from a data block on the disc of Kobayashi because all of the information read from the disc, which would include header information, is synthesized. Honma further discloses that recovered data is phase shifted by

time-delaying the recovered data (Col. 5, lines 27-35) and teaches that by time-delaying the recovered data, the amplitude of fluctuation can be detected (Col. 5, lines 24-27).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to phase shift the recovered data in the method and apparatus of Kobayashi by time-delaying the recovered data as taught by Honma, the motivation being to allow for detection fluctuation amplitude.

5. Claims 11 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi in view of Horigome (US 5,682,374).

Kobayashi discloses the method and apparatus for reading a block of data from an optical disc wherein a read clock is used to recover the data; and wherein the recovered data is phase shifted by creating a phase difference between the read clock and the recovered user data as claimed in claims 1, 9, 16, and 21. Kobayashi does not disclose that the recovered data is phase shifted by time-delaying the read clock.

Horigome discloses a method and apparatus for reading a block of data from an optical disc wherein a read clock is used to recover the data; and wherein the recovered data is phase shifted by creating a phase difference between the read clock and the recovered user data (Fig. 11 and Col. 16, lines 54-58). Horigome further discloses a phase adjustment circuit (Fig. 11, element 44) that comprises delay circuits (Fig. 11, elements 51 and 61) for time-delaying the read clock (Fig. 11, SMPLCLK) to shift the phase of the recovered user data. Horigome teaches adjusting the phase of the read clock to allow for reproduction from a higher density recording.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to time-delay the read clock in the method and apparatus of Kobayashi to

phase shift the recovered data as suggested by Horigome, the motivation being to reproduce data from a high density recording.

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi in view of Tanoue et al (hereafter Tanoue) (US 6,091,688).

Kobayashi discloses a method for reading a block of data from an optical disc as claimed in claim 1. Kobayashi does not disclose that the recovered user data is stored in memory prior to demodulation; and wherein the recovered user data is digitally phase-shifted by shifting the data stored in the memory.

Tanaoue discloses a method for reading a block of data from an optical disc, wherein actual header information and user data are recovered form the disc. Tanoue further discloses that the recovered user data is stored in memory prior to demodulation; and wherein the recovered user data is digitally phase-shifted by shifting the data stored in the memory (Fig. 15, elements 74 and 75). The examiner notes that the data stored in the memory of Tanoue will inherently be digitally phase-shifted because the memory is a shift register. Tanoue teaches that storing the data in memory will allow the serial data to be converted to parallel data to be operated on by the demodulation circuit (Col. 16, lines 48-52).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to store user data from the circuit of Kobayashi in memory prior to demodulation and to digitally phase shift recovered user data in the memory, the motivation being to convert the recovered user data to parallel data to be operated on by the demodulation circuit.

7. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi in view of Tsuyoshi et al (hereafter Tsuyoshi) (US 4,748,611).

Kobayashi discloses the method for reading a block of data from an optical disc as claimed in claim 1. Kobayashi does not disclose that a phase difference between synthesized and recovered header information is determined for only the first data sector of the block.

Tsuyoshi discloses a method for reading a block of data from an optical disc wherein a phase difference is determined for only the first data sector of the block (Fig. 5A and Col. 8, lines 8-21) and teaches that having header information, including address and synchronization information only at the beginning of each data block will raise data capacity of the disc (Fig. 5A and Col. 3, line 68-Col. 4, line 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to determine a phase difference between synthesized and recovered header information in the method of Kobayashi for only the first data sector of the block as suggested by Tsuyoshi, the motivation being to raise the data capacity of the disc.

8. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi in view of Tsuyoshi.

Kobayashi discloses the apparatus for reading a block of data from an optical disc as claimed in claim 16. Kobayashi further discloses a read clock used by the data recovery unit; and wherein the phase difference is inherently faded towards zero according to a time constant related to the read clock by the second circuit (Col. 8, line 65 - Col. 9, line 13). The examiner notes that the phase of clock signal produced by the PLL circuit cannot be instantaneously changed to compensate for a phase difference between the output of the mark detection circuit and the output of the divider. Therefor, the compensation occurs gradually as the phase difference is faded to zero. Kobayashi does not disclose that the second circuit determines a phase difference only for the first data sector of the block.

Tsuyoshi discloses a method for reading a block of data from an optical disc wherein a phase difference is determined for only the first data sector of the block (Fig. 5A and Col. 8, lines 8-21) and teaches that having header information, including address and synchronization information only at the beginning of each data block will raise data capacity of the disc (Fig. 5A and Col. 3, line 68-Col. 4, line 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the second circuit of Kobayashi to determine a phase difference between synthesized and recovered header information for only the first data sector of the block as suggested by Tsuyoshi and then to fade the phase difference to zero according to a time constant related to the read clock, the motivation being to raise the data capacity of the disc.

9. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi in view of Hikima (US 6,091,682).

Kobayashi discloses the apparatus of 16 wherein the apparatus is an optical disc drive (Col. 1, line 10). Kobayashi does not disclose that optical disc drive is a DVD drive.

Hikima discloses that DVD's have a higher recording density than CD's and that DVD's have prerecorded synchronization information (Col. 1, lines 7-15).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the optical disc drive of Kobayashi a DVD drive as suggested by Hikima, the motivation being to increase recording density by using a high density optical disc.

Citation of Relevant Prior Art

10. Yamamoto et al (US 6,577,569) discloses a method of reading a block of data stored on an optical disc, the data block including header information, the method comprising the steps of:

synthesizing header information for the data block; recovering actual header information from the disc; and recovering actual user data from the disc, the user data being phase shifted by a phase difference between the synthesized header information and missing recovered header information (Figs. 1 and 2). Watanabe et al (US 6,198,718) discloses synthesizing a wobble and address signal to be recorded on an optical disc (Fig. 2). Saito et al (US 5,233,589) discloses a reproduced data synthesizing means that reconstructs first and second reproduced signals while correcting edge shifts produced during data recording by storing the reproduced signals in memory (Col. 3). Wada (US 4,931,628) discloses a synthesis means that synthesizes address data (Cols. 16-17). Yokogawa et al (US 5,440,532) discloses a sample clock that is synchronized with the phase of a read signal by phase correcting based on a difference in phase between two samples (Fig. 4). Shim (US 6,333,902) discloses using a wobble header signal to count down sectors to a last sector of a track and thereby synthesizes address information from a header.

Allowable Subject Matter

11. Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

12. Applicant's arguments filed January 20, 2004 with respect to the rejections of the claim 1 as being anticipated by Kobayashi (US 5,835,461) have been fully considered but they are not persuasive.

In regard to Applicant's arguments that Kobayashi uses an edit buffer which is avoided by the method of claim 1, see Page 8, line 22-Page 9, line 3, it is noted that the method of claim 1 does not require the use of an edit buffer to be avoided. Therefore, Applicant's argument is not relevant to the rejection of claim 1.

In regard to Applicant's arguments, see Page 9, line 5-Page10, line 3, that Kobayashi does not teach user data being shifted by a phase difference between synthesized and recovered header information, Applicant states that the phase difference detected by the comparator of Kobayashi (Fig. 14, element 42) is not used to shift user data and is not between synthesized and recovered header information. The phase difference detected by the comparator is used to shift user data because the phase difference is used to adjust or shift the phase of the clock used to reproduce user data from an optical disc. The shift in the reproduction clock causes user data, which is read with the reproduction clock, to be shifted. In addition, the phase difference detected by the comparator is between synthesized and recovered header information. The sync marks are interpreted as header information. The mark cycle detection circuit (Fig. 14, element 40) generates pulses in synchronization with detected sync marks and supplies them to the phase comparator if the detected sync marks have constant period (Col. 8, lines 55-60). The phase comparator is part of a phase lock loop (PLL) circuit (Fig. 14, element 41). The PLL adjusts the phase of a clock used for reproduction to have the phase of the pulses generated by the mark cycle detection circuit. Therefore, if the detected sync marks have constant period, the phase of the PLL output matches the phase of the detected sync signals or detected header information. When the detected signals no longer have constant period, the mark cycle detection circuit generates pseudo pulses to replace the pulses synchronized and in phase with the detected sync marks (Col. 8, lines 60-62). The pseudo pulses are interpreted as synthesized sync marks and as a result,

synthesized header information. Thus, when the detected sync marks or detected header information no longer in constant period, the phase of the first pseudo pulse or synthesized header information generated is compared with the phase of the divided PLL output, which is synchronized to the phase of detected header information. The resulting phase difference between synthesized and detected header information shifts user data that is recovered from the disc by adjusting the phase of the reproduction clock.

13. Applicant's arguments filed January 20, 2004 with respect to the rejections of claims 15, 16, and 26 as being anticipated by Kobayashi have been fully considered but they are not persuasive. Applicant's argument that Kobayashi does not meet claims 15, 16, and 26 for the same reasons that Kobayashi does not meet claim are not persuasive for the reasons stated above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael V Battaglia whose telephone number is (703) 305-4534. The examiner can normally be reached on 5-4/9 Plan with 1st Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoa T Nguyen can be reached on (703) 305-9687. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael Battaglia

W. R. YOUNG
PRIMARY EXAMINER